Innoscience 英诺赛科

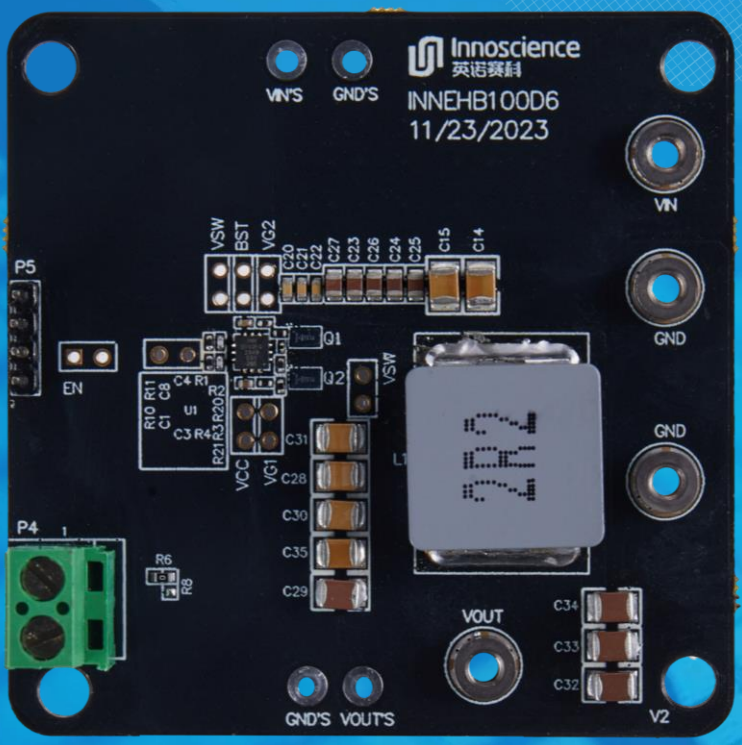
POWER THE FUTURE

INNEHB100D6

Evaluation Board Manual

100V Half-Bridge GaN Driver

INS2002 EVB



CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by

ELECTRICAL SHOCK HAZARD

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.

Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

HOT SURFACE

The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

REMINDER

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

List of Content

1. Overview

1.1. Introduction

INNEHB100D6 is a half-bridge evaluation board equipped with two 100V,7mΩ GaN FETs to evaluate the performance of INS2002 100V half-bridge driver for enhancement-mode GaN FETs. This board can simplify the test process, it can easily realize Buck or Boost converter with single PWM input. The board includes all the necessary information you need, and the layout has been optimized to achieve the best performance. Test points are also included for the waveform measurement and efficiency evaluation. This board is not intended to be used as a standalone product, but rather for evaluating the performance of INS2002.

1.2. Test Equipment Requirement

To evaluate the performance properly, you need to prepare the following test equipment:

1) High speed digital oscilloscope (≥500MHz Bandwidth)
2) 300W Low voltage DC power supply
3) PWM generator
4) Digital Multimeter
5) DC load (E-load or Power Resistor)

2. Performance Summary

Table 1 Electrical Characteristic (Ta=25℃)

Symbol	Parameters	Min	Nom	Max	Units
VDD	Gate Drive Regulator Supply Range	6		12	V
Vin	Input Voltage			80(1)	V
Pout	Output Power			250(2)	W
Vpwm(3)	Input Logic 'High'	3.5		5	V
	Input Logic 'Low'	0		1.5	V

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 100 V.

(2) Maximum output power depends on die temperature – actual maximum output power with be subject to switching frequency, bus voltage, load current and thermal cooling.

(3) The PWM input threshold here is the logic gate on the EVB, not INS2002

3. Block Diagram

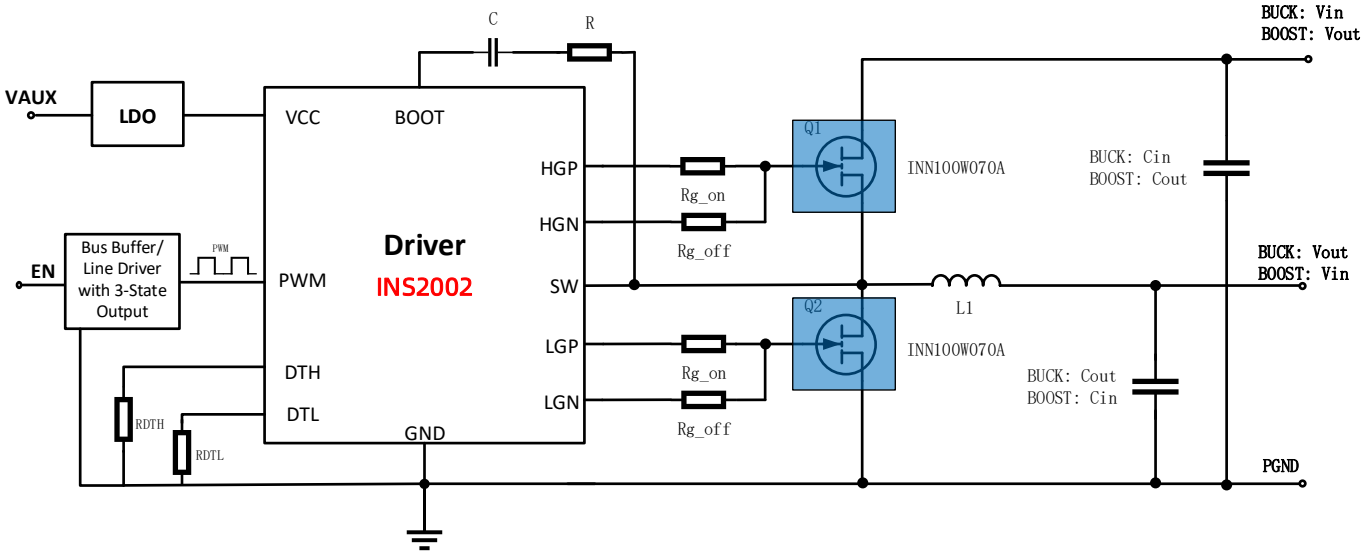


Figure 1 INNEHB100D6 Block Diagram

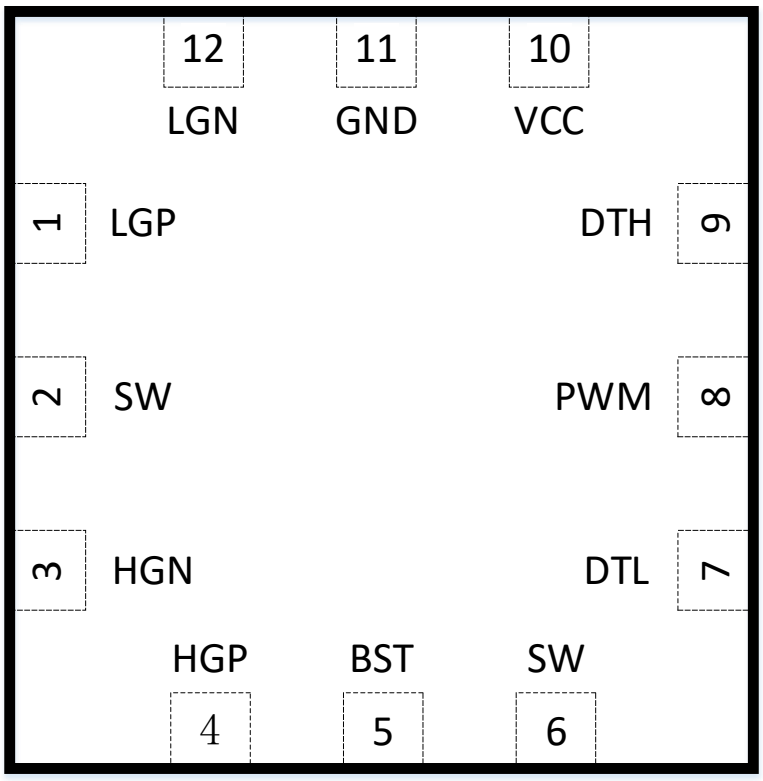


Figure 2 12-Lead FC-QFN(3mm×3mm) Package

Features:

1. Single PWM Input with Three PWM Input States: High, Low, and Tri-State.
2. Split Outputs for Adjustable Turn-on/-off Speeds.
3. Strong 1-Ω Pullup and 0.2-Ω Pulldown Resistance.
4. Internal Strong and Smart Bootstrap Switch.
5. Adjustable Dead Time Optimized for GaN FETs.
6. Adaptive Shoot-Through Protection.
7. Fast Propagation Delay (22ns Typical).
8. High-Side Floating Supply Operates up to 80V DC.

4. PCBA Overview and Schematic

4.1. PCBA Overview

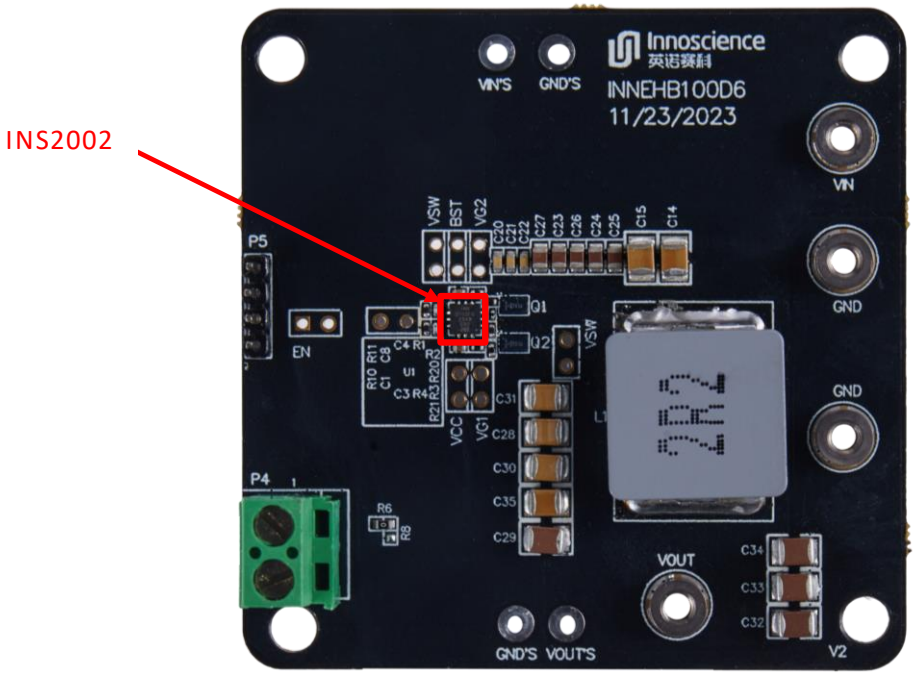


Figure 3 Top view of INNEHB100D6

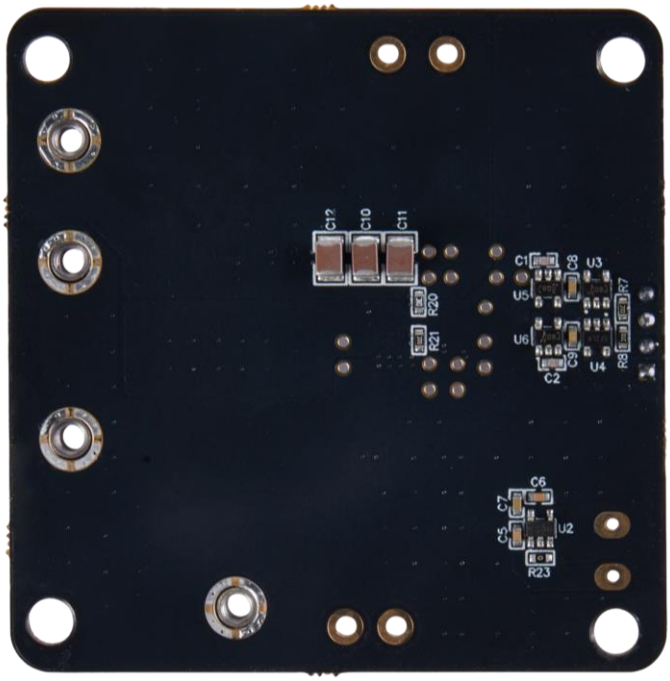
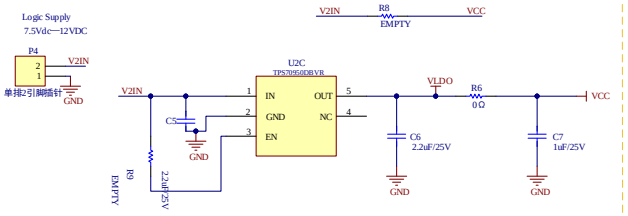
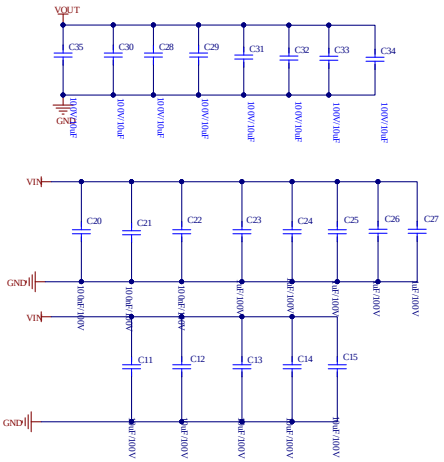


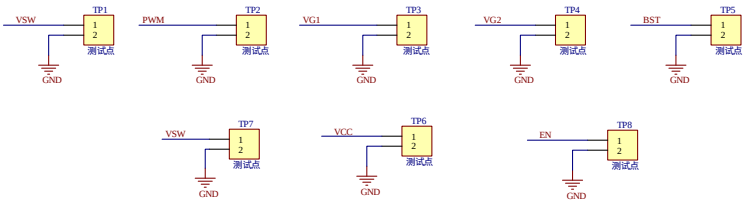
Figure 4 Bottom view of INNEHB100D6

4.2. Schematic



LDO辅助供电





半桥功率电路

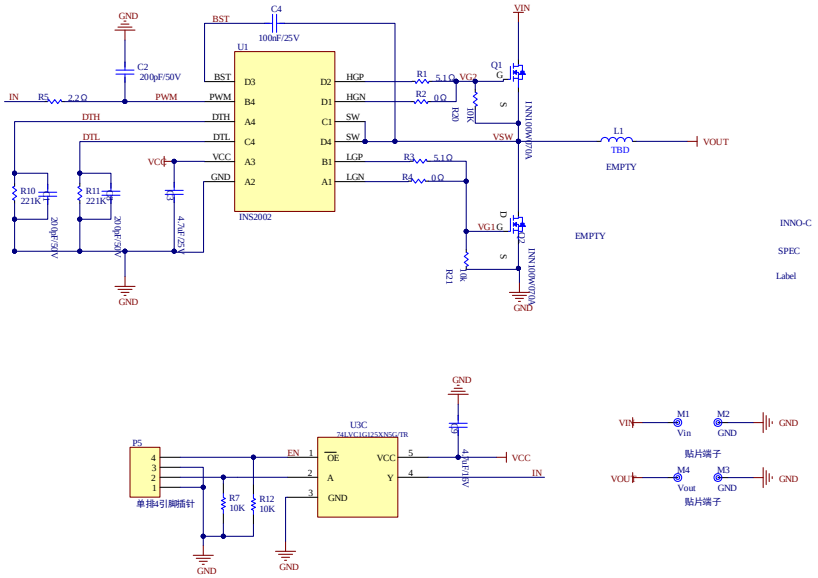


Figure 5 Schematic

5. Testing Guide

5.1. Test point location

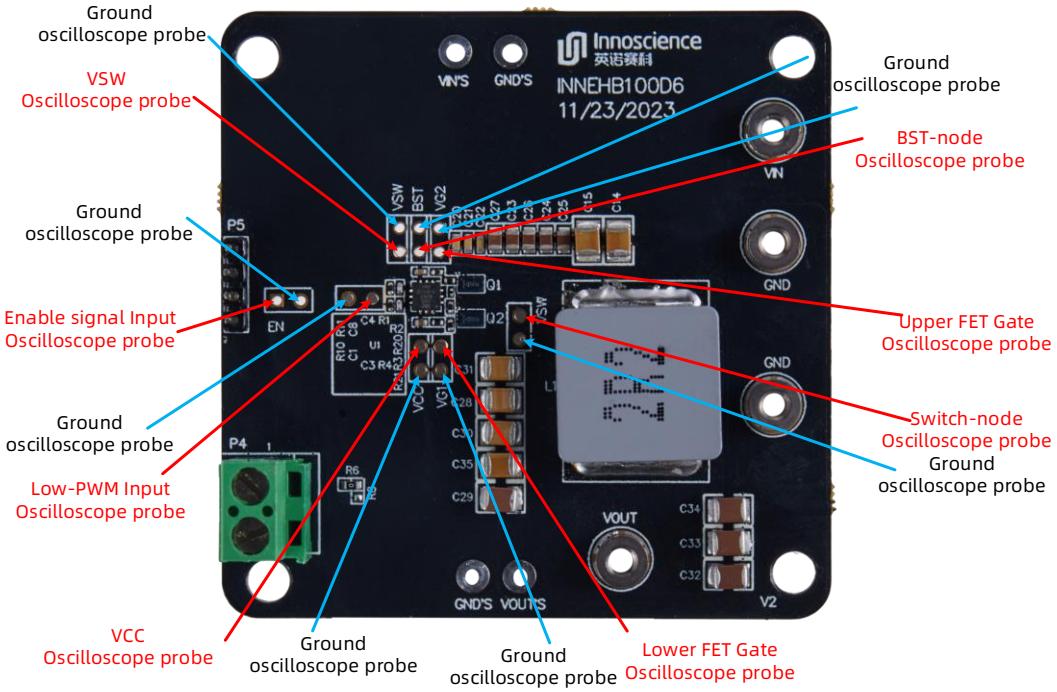


Figure 6 Measurement points

5.2. Test setup

5.2.1. Buck Mode

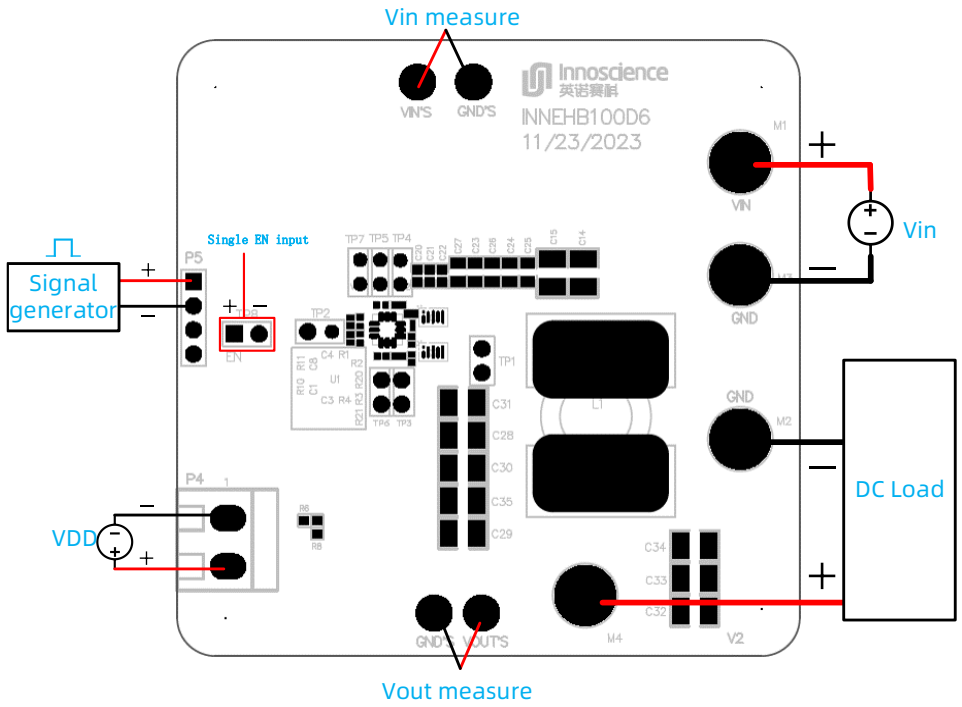


Figure 7 Single-PWM input Buck mode

The driver of the EVB has a single input to control high-side and low-side drivers in three states: High, Low, and Tri-State, and the driver has split outputs to adjust turn-on and turn-off speeds separately. Independent dead time can be adjusted through external resistors R10 and R11. The default value for R10 and R11 is 220Ω. The value of C1 and C8 is 220 pF. At this time, the corresponding measured dead time between lower FET shutdown and upper FET opening is 10ns, and the dead time between upper FET shutdown and lower FET opening is also 10ns.

5.2.2. Boost Mode

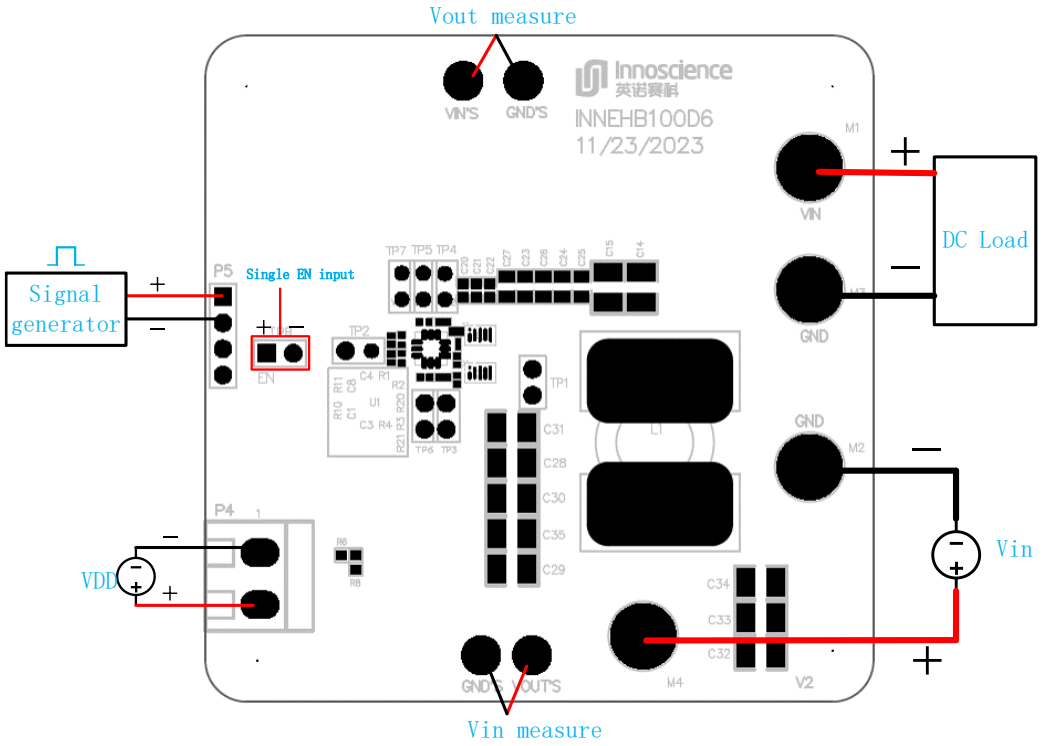


Figure 8 Single-PWM input Boost mode

5.3. Power up and down sequence

5.3.1. Power-up sequence (Buck Mode)

1. Check every power supply is **off.**
2. Connect the DC voltage source to VIN terminal and common ground GND terminal, as shown in Figure 6 (Pay attention to the polarity).
3. Connect the electronic load to VOUT terminal and common ground GND.
4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).
5. Connect the signal generator to pin **P5**.
6. **Turn on the auxiliary power supply.** Note the voltage ranges from 6V ~ 12V.
7. **Turn on the signal generator** with the required duty ratio and frequency .
8. Under no-load conditions, **turn on the bus power supply and slowly increase the voltage to the desired value** (do not exceed the absolute

maximum voltage). Probe switch-node and view the switching operation.

9. **After the output voltage is established normally, then add the load current,** do not exceed the maximum temperature required by the device specification.

5.3.2. Power-up sequence (Boost Mode)

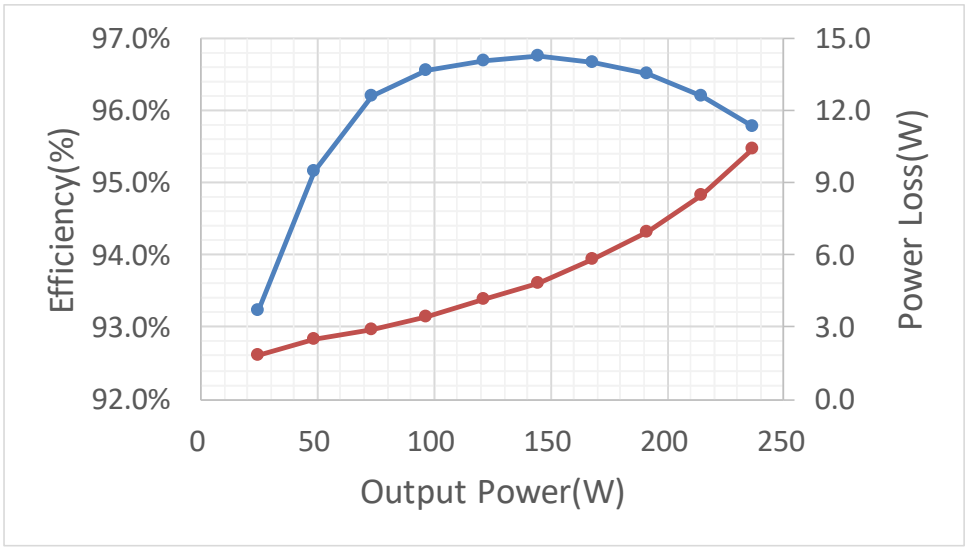
1. Check every power supply is **off**
2. Connect the DC voltage source to VOUT terminal and common ground GND terminal, as shown in Figure 8 (Pay attention to the polarity).
3. Connect the electronic load to VIN terminal and common ground GND terminal, as shown in Figure 8 (Pay attention to the polarity).
4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).
5. Connect the signal generator to pin **P5**.
6. **Turn on the auxiliary power supply**. Note the voltage ranges from 6V ~ 12V.
7. **Turn on the signal generator** with the required duty ratio and frequency.
8. Under no-load conditions, **turn on the bus power supply and slowly increase the voltage to the desired value** (do not exceed the absolute maximum voltage). Probe switch-node and view the switching operation.
9. **After the output voltage is established normally, then add the load current,** do not exceed the maximum temperature required by the device specification.
10.

5.3.3. Power-down sequence

1. Turn off the **E-load** first
2. Turn off the **Bus power supply**
3. Turn off the **PWM generator**
4. Turn off the **auxiliary power supply**

6. Evaluation Results

6.1.1. Efficiency Results



Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

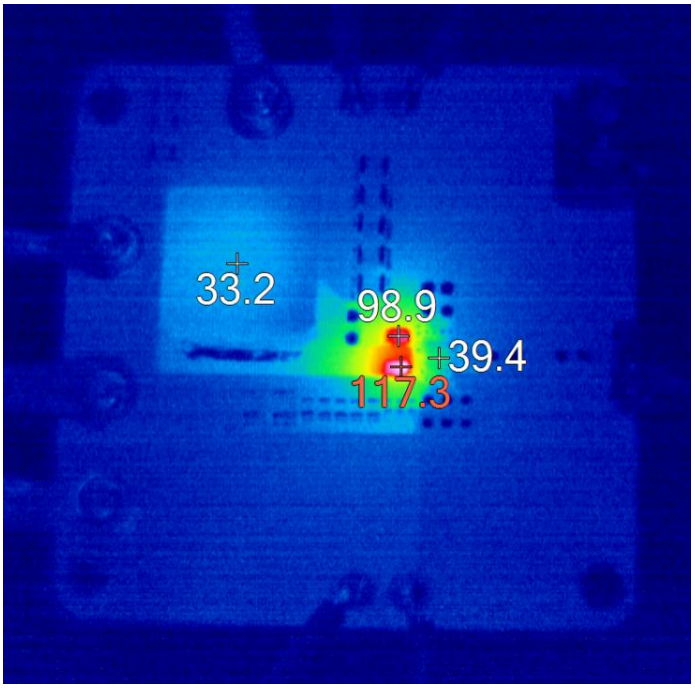
fsw=600kHz

Airflow=1400LFM

Rg_on=5.1Ω

Rg_off=0Ω

6.1.2. Thermal performance



Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

Iout=20A

fsw=600kHz

Airflow=1400LFM

Rg_on=5.1Ω

Rg_off=0Ω

Result

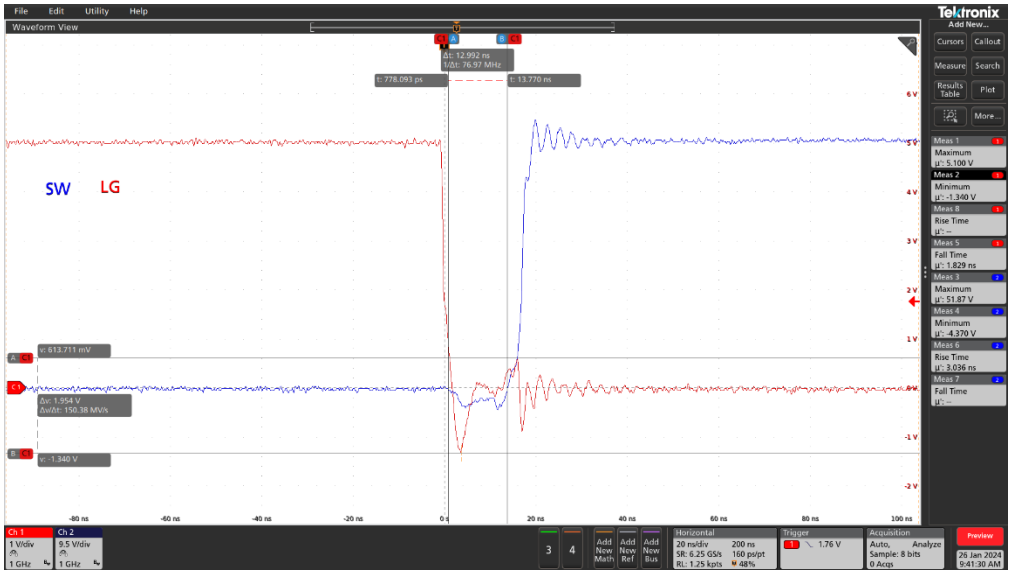
Driver INS2001: 39.4℃

Switching GaN: 117.3℃

Continuation GaN: 98.9℃

Inductor: 33.2℃

6.1.3. Switching Waveforms



Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

Iout=20A

fsw=600kHz

Airflow=1400LFM

Rg_on=5.1Ω, Rg_off=0Ω

Result

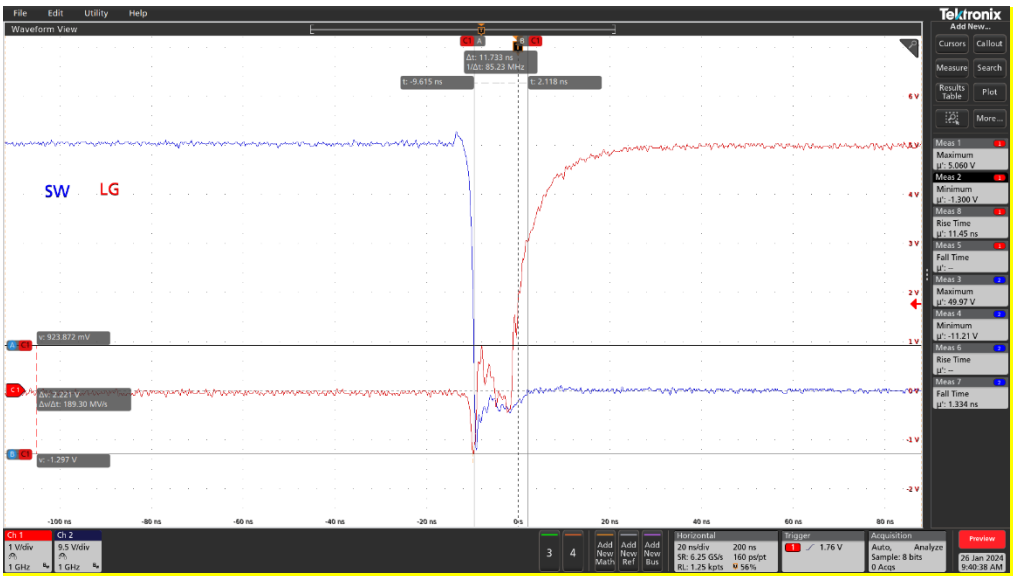
SW Edge:

Falling Time=3.036ns

Falling Overshoot=-1.34V

LG Edge:

Rising time=3.036ns,



Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

Iout=20A

fsw=600kHz

Airflow=1400LFM

Rg_on=5.1Ω, Rg_off=0Ω

Result

SW Edge:

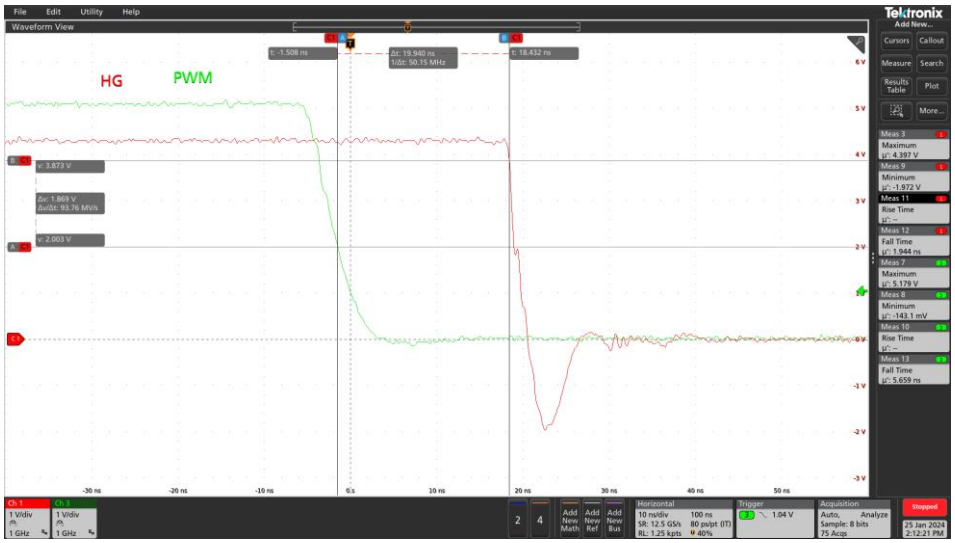
Rising Time=11.45ns

Rising Overshoot =1.97V

LG Edge:

Falling time=1.334ns

6.1.4. Delay time



Test conditions

Buck Mode

Vin=0Vdc

Vout=5Vdc

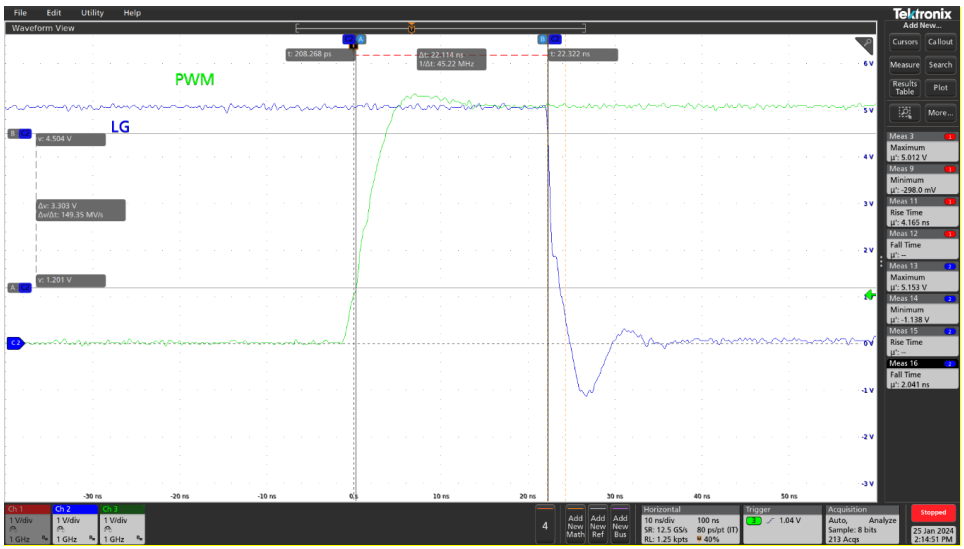
fsw=600kHz

Airflow=1400LFM

Rg_on=5.1Ω, Rg_off=0Ω

Result

PWM falling to Vgs_h falling delay time: 20ns



Test conditions

Buck Mode

Vin=0Vdc

Vout=5Vdc

fsw=600kHz

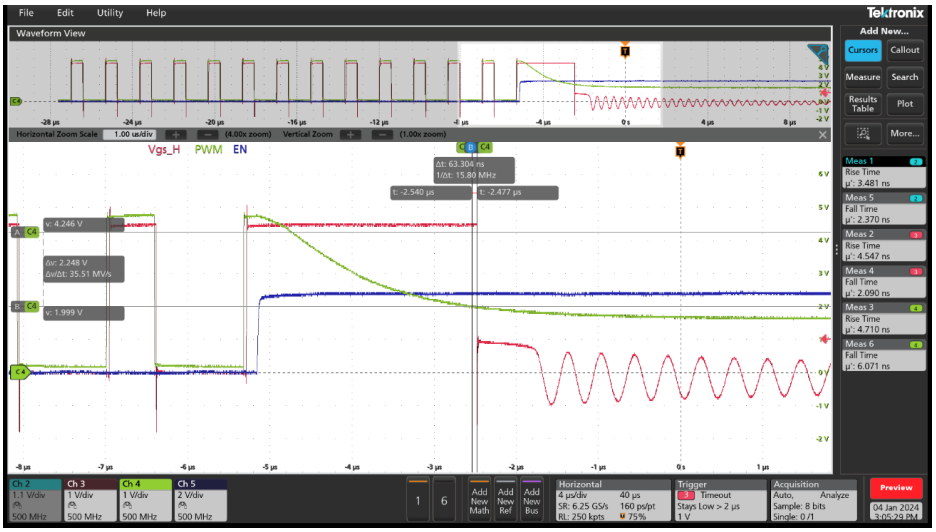
Airflow=1400LFM

Rg_on=5.1Ω, Rg_off=0Ω

Result

PWM rising to Vgs_L falling delay time: 22ns

6.1.5. Tri_State transition



Test conditions

Buck Mode

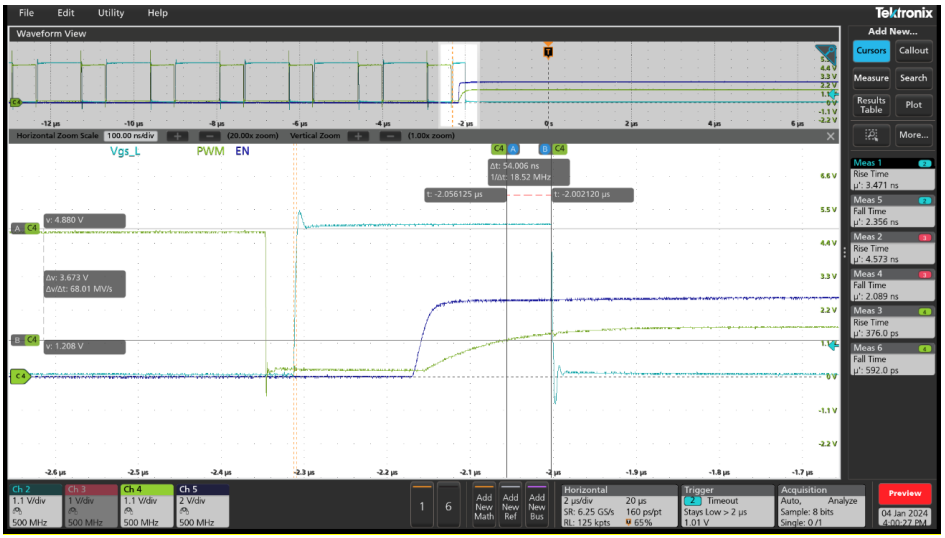
Vin=0Vdc

Vcc=5Vdc

Duty=34.9%

fsw=600kHz

Rg_on=Rg_off=0Ω



Test conditions

Buck Mode

Vin=0Vdc

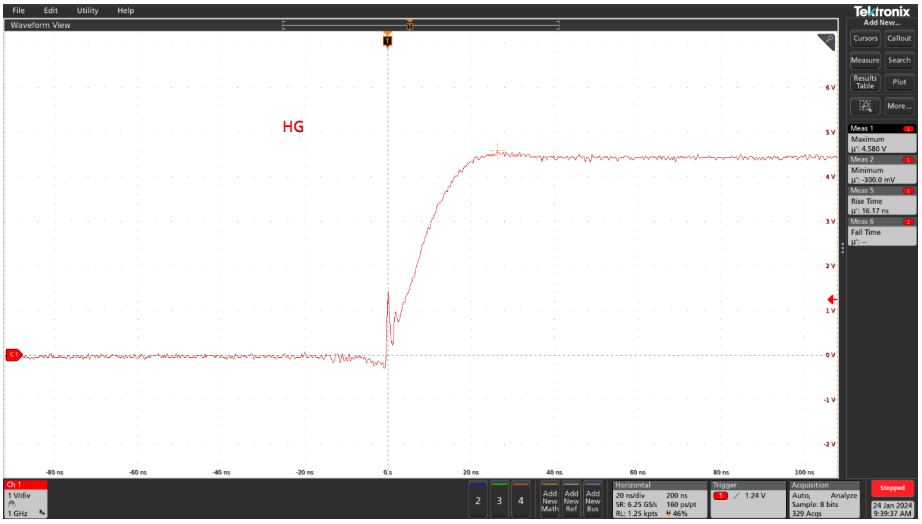
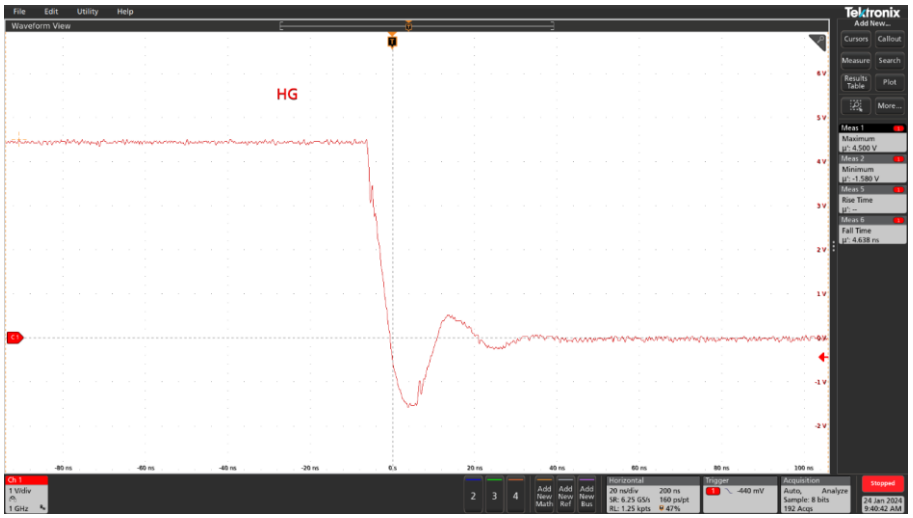
Vcc=5Vdc

Duty=34.9%

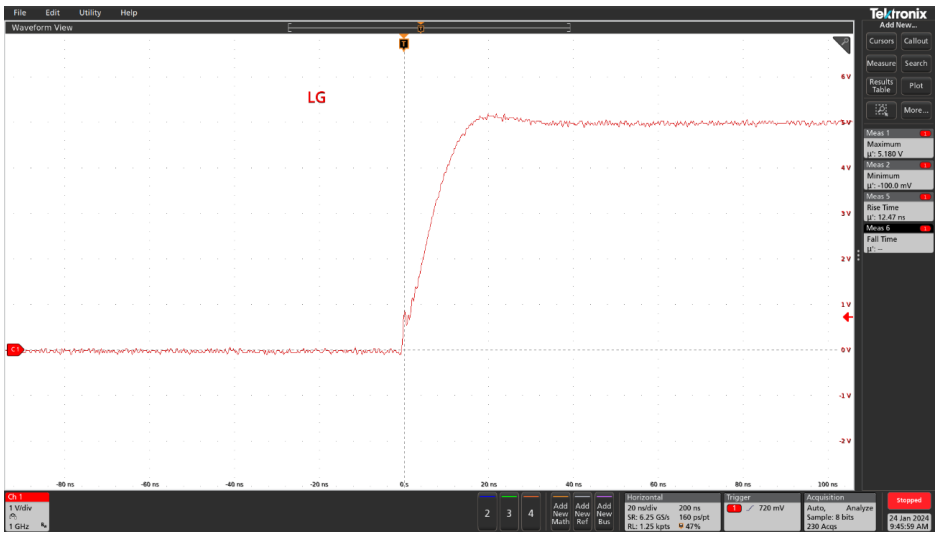
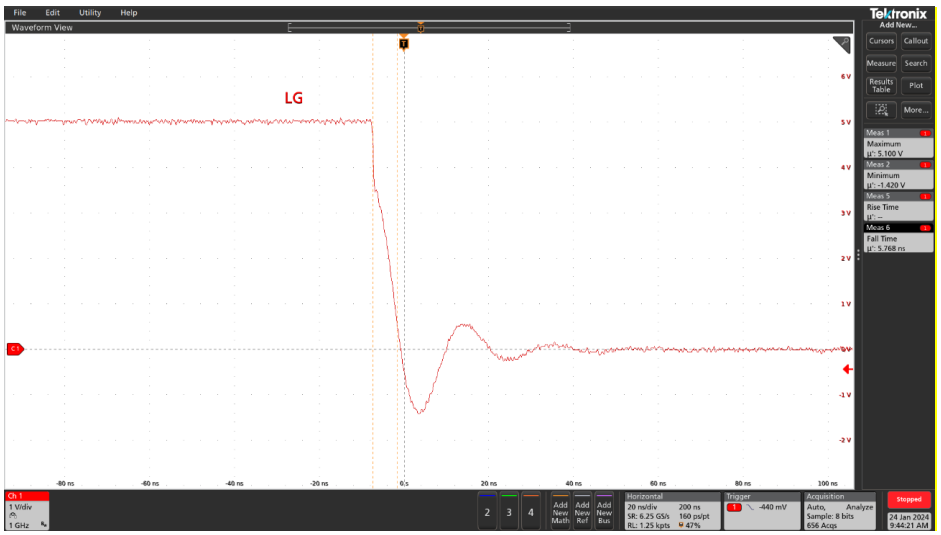
fsw=600kHz

Rg_on=Rg_off=0Ω

6.1.6. High Side Gate Output Rise/Fall Time

	**Test conditions** **Load:3.3nF//INN100W070A** **Result** Rise Time： 16.2ns
	**Test conditions** **Load:3.3nF//INN100W070A** **Result** Fall Time： 4.6ns

6.1.7. Low Side Gate Output Rise/Fall Time

	**Test conditions** **Load:3.3nF//INN100W070A** **Result** **Rise Time: 12.5ns**
	**Test conditions** **Load:3.3nF//INN100W070A** **Result** **Fall Time: 5.8ns**

Appendix

Appendix A. PCB Layout

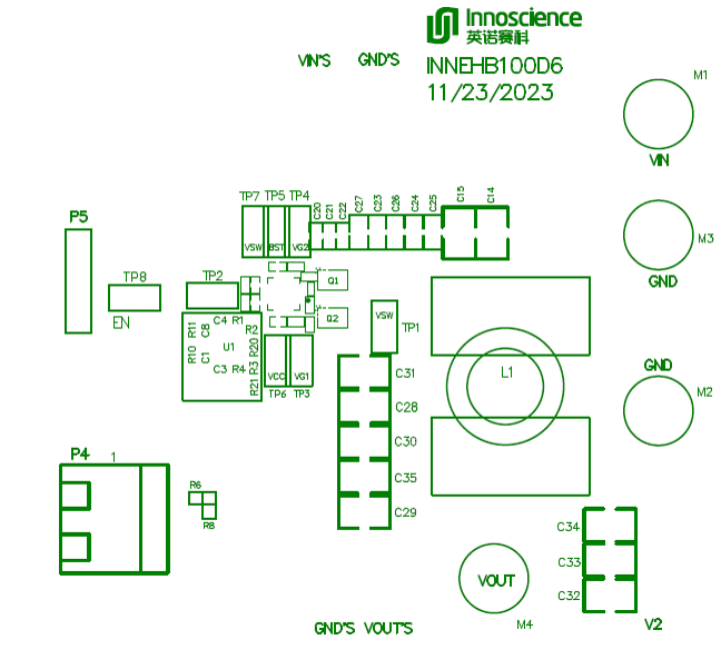


Figure 9 The top overlay of INNEHB100D6

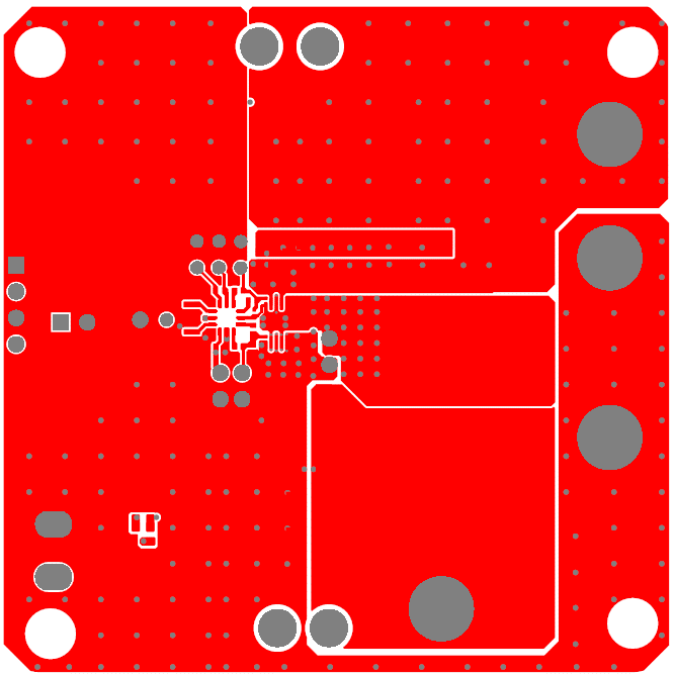


Figure 10 The top layer of INNEHB100D6

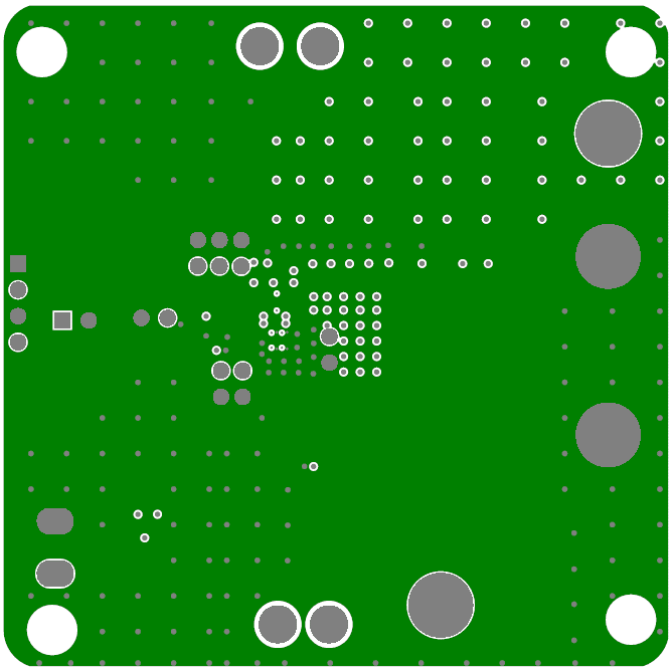


Figure 11 The first middle layer of INNEHB100D6

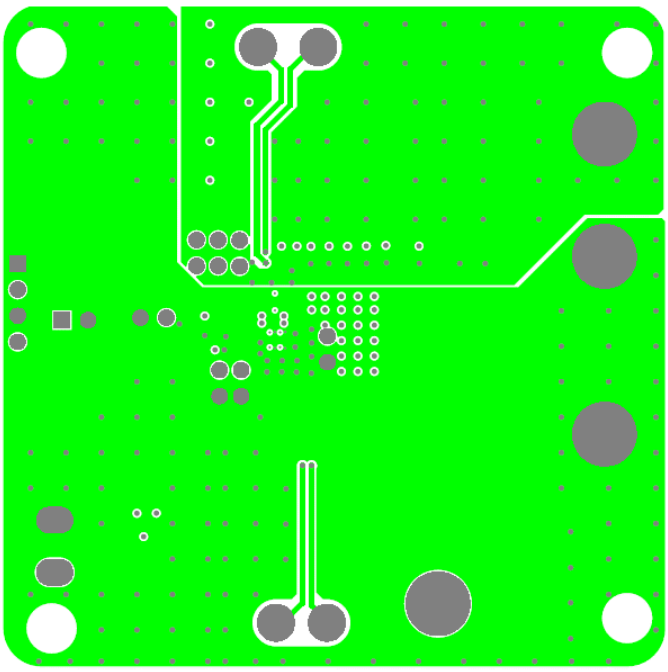


Figure 12 The second middle layer of INNEHB100D6

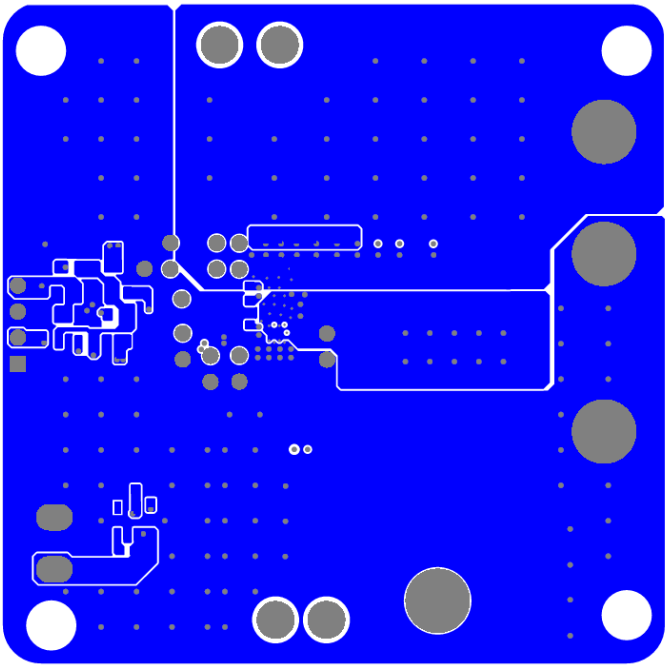


Figure 13 The bottom layer of INNEHB100D6

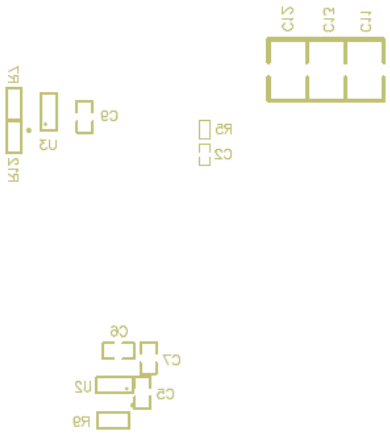


Figure 14 The bottom overlay of INNEHB100D6

Appendix B. BOM

Table 2 BOM

Designator	Part Number	Manufacturer	Description	Footprint	Quantity
C1, C2, C8	0402N201J500CT	Walsin	CAP, 200pF/50V, ±5%, C0G	C0402	3
C3	TMK107BBJ475KA-T	TAIYO YUDEN	CAP, 4.7uF/25V, ±10%, X5R	C0603	1
C4	CGA2B3X7R1E104KT0Y0F	TDK	CAP, 100nF/25V, ±10%, X7R	C0402	1
C5, C6	CC0603KRX5R8BB225	YAGEO	CAP, 2.2uF/25V, ±10%, X5R	C0603	2
C7	TMK107BJ105KA-T	TAIYO YUDEN	CAP, 1uF/25V, ±10%, X5R	C0603	1
C9	CC0603KRX7R8BB104	YAGEO	CAP,100nF/25V, ±10%, X7R	C0603	1
C23, C24, C25, C26, C27	GCM21BC72A105KE36L	muRata	CAP,1uF/100V, ±10%, X7S	C0805	5
C11, C12, C13, C14, C15, C28, C29, C30, C31, C32, C33, C34, C35	GRM32EC72A106KE05L	muRata	CAP,10uF/100V, ±10%, X7S	C1210	13
C20, C21, C22,	CL10B104KC8NNNC	SAMSUNG	CAP,100nF/100V, ±10%, X7R	C0603	3
L1	MWLA1707S-2R2MT	Sunlord	Inductance, 2.2uH, DCR: 2.7mΩ,	17*17.5*6.6mm	1
Q1, Q2	INN100W070A	Innoscience	GAN FETs, 100V/7mΩ, Innoscience	WLCSP 2.5×1.5mm	2
R1, R3	HQ02WAF510KTCE	UNI-ROYAL	Chip resistors, 5.1Ω, 100mW, 0402	0402	2
R2, R4	HP02WAJ0000TCE	UNI-ROYAL	Chip resistors, 0Ω, 100mW, 0402	0402	2
R5	RC-02U2R20FT	FH	resistance, 2.2Ω, ±1%, 0402	0402	1
R6	ERJ3GEY0R00V	PANASONIC	Chip resistors, 0Ω, 100mW, 0603	R0603	1
R7, R12	ERA3AEB103V	PANASONIC	Chip resistors, 10KΩ, ±0.1%, 0603	R0603	2
R8, R9	EMPTY		Chip resistors, EMPTY, 0603,	R0603	2
R10, R11	RTT022213FTH	RALEC	Chip resistors, 220kΩ, ±1%, 0603	R0603	2
R20	0201WMF1002TEE	UNI-ROYAL	Chip resistors, 10kΩ	R0201_M	1
R21	0402WGF1002TCE	UNI-ROYAL	Chip resistors, 10kΩ	R0402	1
U1	INS2002FQ	Innoscience	Single-Channel Gate Driver	FCQFN 3*3mm	1
U2	TPS70950DBVR-TP	TECH PUBLIC	LDO voltage regulators , fixed 5V output,	SOT-23	1
U3	74LVC1G125XN5G/TR	SGMICRO	Bus Buffer/Line Driver with 3-State Output	SOT-23-5	1

Revision History

Date	Versions	Description	Author
2024/07/19	1.0	First edition	AE Team

Note:

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